North Maharashtra University, Jalgaon

New Syllabus with effect from Year 2006-07

SE Computer Term I

Sr. No	Subject	Teaching Scheme per Week			Examination Scheme				
		L	T	P	Paper Hr.	Paper	TW	PR	OR
1	Analog Electronics	4	-	2	3	100	25	25	-
2	Discrete Structure and Graph Theory *	4	-	-	3	100	-	-	-
3	Digital Systems and Microprocessor *	4	-	2	3	100	50	25	-
4	Industrial Management and Economics *	4	-	-	3	100	-	-	-
5	Engineering Mathematics III *	4	1	-	3	100	25	-	-
6	Programming Laboratory I *	3	-	4	-	-	50	50	-
	Total	23	1	8		500	150	100	-
	Grand Total	**32**			**750**				

SE Computer Term II

Sr. No	Subject	Teaching Scheme per Week			Examination Scheme				
		L	T	P	Paper Hr.	Paper	TW	PR	OR
1	Microprocessor I *	4	-	2	3	100	25	25	-
2	Data Structure and Files *	4	-	4	3	100	50	50	-
3	Computer Organization *	4	-	-	3	100	-	-	-
4	Digital System Design	4	-	-	3	100	-	-	-
5	Data Communication *	4	-	-	3	100	-	-	-
6	Programming Laboratory II *	2	-	4	-	-	50	50	-
	Total	22	0	10		500	125	125	-
	Grand Total	**32**			**750**				

* Common subject with SE IT

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SE (COMPUTER ENGINEERING)
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TERM – I

ANALOG ELECTRONICS

Teaching Scheme:
Lectures: 4 Hrs / Week
Practical: 2 Hrs / Week

Examination Scheme:
Theory Paper: 100 Marks (3 Hrs)
Term work: 25 Marks
Practical: 25 Marks

Unit – I

Basic Definition, ideal and practical voltage and current sources, dependent and independent voltage and current sources, Linear, unilateral, bilateral networks.
Loop and node analysis (DC & AC).
Network Theorems – (AC & DC) (including controlled sources) superposition, Thevenin's and Norton's and Maximum power theorem, principle of duality.

(10 Hrs, 20 Marks)

Unit – II

Transistor at low frequencies: Analysis of an amplifier using h-parameters $A_{I,}$ R_i , A_V, A_{VS}, A_{IS}, R_O.
CE, CB, CC configurations, Miller's theorem, Miller's Dual theorem.
Transistor at high frequencies: CE hybrid Π-model, significance, CE short circuit current gain and current gain with resistive load.

(10 Hrs, 20 Marks)

Unit – III

Cascade Configurations – CE-CE, CE-CB, CE-CC, CC-CC (Darlington pair), Bootstrapping, Emitter coupled differential amplifier (DC analysis and AC analysis for Ad, Ac and CMRR using h-parameters), square wave testing.
Large signal amplifier: Class A – Direct coupled, Transformer coupled, Class A push-pull, Harmonic distortion.

(10 Hrs, 20 Marks)

Unit – IV

FET biasing: JFET and MOSFET biasing (Q point). Low frequency analysis CS configurations
Feedback amplifier: Classification, block diagram of general feedback concept (Negative), Relation between A_F and A, Block diagram of A feedback amplifier topologies, General characteristics and advantages of negative feedback amplifier.
Oscillator: Barkhausain criterion, Phase shift oscillator, Wein bridge oscillator, Collpits oscillator, Hartley oscillator, Clapp oscillator (no derivations).

(10 Hrs, 20 Marks)

Unit – V

Voltage Regulators:
Performance parameters of regulators; Zener shunt, transistor shunt, emitter follower type series regulator and controlled transistor regulators. (Analysis of Sv and Ro)
Protection circuits: Short-circuit protection, current limiting and feedback current limiting
IC Regulators: Block diagram of 3 PIN IC regulators, LM317, 340 for fixed voltage, adjustable output and current regulator IC723 for low voltage and high voltage as well as current boosting.
SMPS and UPS (Block diagram and working only)

(10 Hrs, 20 Marks)

List of experiments -

1. Study of Superposition and Thevenin's theorem
2. Square wave testing of an amplifier.
3. To plot the frequency response of single stage CE amplifier.
4. To measure mid-band voltage gain of CE from transistor stage followed by CC stage.
5. Find CMRR of Emitter coupled differential amplifier.
6. Push Pull class B power amplifier cross over distortion & its elimination.
7. To calculate the mid-band voltage gain of single stage FET amplifier.
8. Study of LC oscillator
9. Study of Crystal oscillator
10. Load regulation of controlled transformer series regulator
11. Adjustable output and current regulation using IC LM377 and 340
12. Study of SMPS

Term work should include minimum 8 (eight) experiments from above list.

Reference Books -

1. Singh "Electronic Devices and Integrated Circuits", Pearson
2. R S Shedha " Electronic Devices and circuits ", S Chand Publications
3. Salivahanan " Electronic Devices and circuits ", TMH
4. Ramakant A. Gaikwad "Op-Amp and Linear Integrated circuits". 3rd" Ed., Pearson
5. M.E.Van Valkenberg, "Network Analysis", Pearson
6. Boylestad, Kishor "Electronic devices and Circuit Theory", Pearson

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TERM – I

DISCRETE STRUCTURE AND GRAPH THEORY

Teaching Scheme: Examination Scheme:
Lectures: 4 Hrs / Week Theory Paper: 100 Marks (3 Hrs)

Unit - I

Sets, Logic and Proofs

Propositions, proposition and logical operations, Conditional Statements, Propositional Calculus, Quantifiers: universal and existential quantifiers, methods of proofs, Set Theory: Set, Combinations of Sets, Finite and Infinite sets, uncountably infinite sets, Mathematical Induction, Principle of inclusion and Exclusion.

Discrete Probability, Information and Mutual information

(10 Hrs, 20 Marks)

Unit - II

Relations, functions, Recurrence Relations

Definitions, properties of Binary relations, Equivalence Relations and partitions, Partial ordering relations and lattice, chains and antichains, Transitive Closure and Warshall's Algorithm.

Functions Definitions, Pigeonhole principle.

Recurrence Relation, Linear Recurrence Relations with constant Coefficients, Homogeneous Solutions, Particular Solutions, total solutions, Solution by the method of generating functions.

(10 Hrs, 20 Marks)

Unit - III

Graphs:- Basic terminology, multigraphs and weighted graph, paths and circuits, shortest path algorithms, Euler and Hamiltonian Paths and circuits, factors of a graph, Planer graph and Kuratowski theorem, graph coloring.

Trees:- Trees, rooted trees, path length in rooted trees, prefix code, binary search trees, spanning trees and cut set, minimum spanning trees, kruskal's and prim's algorithms for minimum spanning tree.

(10 Hrs, 20 Marks)

Unit - IV

Analysis of Algorithm and Algebraic systems - Time Complexity of algorithms, shortest path algorithms, complexity of problems, tractable and intractable problem.

Algebraic system - Groups, subgroups, Isomorphisms and Automorphisms, Homomorphisms and Normal subgroup, Rings, Integral domains and fields.

(10 Hrs, 20 Marks)

Unit - V

Boolean algebra - Lattice and Algebraic systems, Principle of duality, basic properties of lattice defined by lattices, distributive and complemented lattices, Boolean lattices and Boolean algebras, Boolean functions and Boolean Expressions.

Binary Number systems- binary, octal, hex conversion. Application of Boolean algebra.

(10 Hrs, 20 Marks)

Reference Books

1. C.L. Liu, " Elements of Discrete Mathematics", 2nd edition, TMH
2. Kenneth H. Rosen, Discrete Mathematics and its Application, 5th edition, TMH
3. Lipschutz, lipson, " Discrete Mathematics", 2nd edition, TMH
4. V. K. Balakrishnan, " Graph Theory", TMH
5. B. Kolman, R. Busby and S. Ross, "Discrete Mathematical Structures" 4th edition, Pearson
6. J. Treamblay, R. Manohar," Discrete Mathematical structures with application to computer science", TMH

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TERM – I

DIGITAL SYSTEMS AND MICROPROCESSOR

Teaching Scheme:
Lectures: 4 Hrs / Week
Practical: 2 Hrs / Week

Examination Scheme:
Theory Paper: 100 Marks (3 Hrs)
Term work: 50 Marks
Practical: 25 Marks

Unit – I

Review of fundamental concepts: Basic gates, universal gates & Exclusive gates. Digital Signal, Positive & Negative logic,

Boolean Algebra: Boolean postulate and Theorems, Examples of realization of Boolean functions using Boolean algebra.

Introduction to digital logic families: DTL, TTL & CMOS

(10 Hrs, 20 Marks)

Unit – II

Combination logic design: Standard representation of logical function, K map representation of logical function, simplification of logical function using K map, for 2, 3 & 4 variables. K map with Don't care condition. Introduction to five and six variable K map with don't care condition. Design of half adder, full adder, half sub tractor, full sub tractor

(10 Hrs, 20 Marks)

Unit – III

Combination logic design examples: Various Example of combinations logic circuit (truth table – K map – circuit diagram) with the help of K map and their implementation with the help of Basic/Universal gates.

Design of multiplexer & Demultiplexer: Design of comparator circuits using logic gates. Design of parity generator & checker circuit using logic gates

Introduction to sequential logic circuit: function of one bit memory cell, Truth table and excitation tables of S – R, JK, D & T Flip – Flop.

(10 Hrs, 20 Marks)

Unit – IV

8085 Microprocessor

Introduction to 8085 Microprocessor - Architecture, functional pin diagram, register model, programming model, Bus architecture

Instruction Set of 8085 - Instruction cycle, fetch operation, execute operation machine timing diagram for op code fetch cycle, memory read, I/O read, memory write, I/O write, various addressing modes, various instruction set such as data transfer group, arithmetic group, logical group, branch group, stack, input, output and machine control group, instruction format, various addressing modes

(10 Hrs, 20 Marks)

Unit – V

8085 assembly programming - Assembly Language, comparison of high level language and assembly language, role of assembler, Assembly language programming of 8085: addition and subtraction of 8 and 16 bit numbers, one's and two's complements of 8 and 16 bit numbers, multiplication and division of 8 and 16 bit numbers, largest and smallest number using array, sorting of numbers using array, finding square from look up table, square root of number, program related to shift and masking operation of 8 and 16 bit numbers.

(10 Hrs, 20 Marks)

List of Experiments

Group A

1. Verification of the truth table of logic gates and verification of De Morgan's theorem.
2. Construction of basic gates using universal gate (NAND / NOR)
3. Construction of half adder & full adder circuit. Implementation of full adder with the help of two half adder circuit & one OR gate.
4. Construction of Half subtractor & full subtractor Circuit.
5. Conversion of Gray to Binary and Binary to gray code.
6. Verification of truth table of multiplexes & flip-flops.

Group B (8085 Assembly Language Programming)

1. Addition and subtraction of 8 and 16 bit numbers
2. Determining maximum and minimum elements in array
3. Verification of look up table for BCD to 7 Segment conversions
4. HEX To BCD and BCD to HEX conversion
5. Arranging the numbers in ascending and descending order
6. Shift and mask off operation of 8 bit number

The term work should include minimum four experiments from Group A and minimum four experiments from Group B.

Reference Books

1. Modern Digital Electronics by R.P. Jain, 3rd Edition, TMH.
2. Digital Logic and Computer Design by M. Morris Mano, Pearson.
3. Fundamentals of Digital Circuits by An Anandkumar, Pearson.
4. Microprocessor and Interfacing, 2nd edition, Douglas V Hall
5. Advanced Microprocessors and Interfacing, B Ram, TMH

6. Microprocessor architecture, programming and applications, 2nd ed, Ramesh Gaonkar
7. Introduction to Switching Theory and Logic Design, Hill and Peterson, John Wiley and Sons.
8. Digital system, James E Palmer, David E Parlman, McGraw Hill.

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TERM – I

INDUSTRIAL MANAGEMENT AND ECONOMICS

Teaching Scheme: Examination Scheme:
Lectures: 4 Hrs / Week Theory Paper: 100 Marks (3 Hrs)

Unit - I
History of Management, Scientific Management, & its Principles, Administration Management, Neo – Classical Theory, Gilberth's contribution, Modern management Theories, Relation between Administration and organization, Levels of managements, Function of Management.

(10 Hrs, 20 Marks)

Unit – II
Organizational structures: Line, functional, Line staff forms of Business ownerships: Proprietorship, partnership Joint stock Co - Pvt. Ltd. Co., public Ltd Co., Co-operative organizations, public sector, joint ventures, Their meanings, formation, Advantage, Limitations & Applications.

(10 Hrs, 20 Marks)

Unit – III
Engineering Economics. Wants, Utility, Demand, Supply, Elasticity of demand & supply. Capital: Fixed, Working capital, sources of finance Credit, shares, Debentures, ploughing Back, Loans from banks, Trade Public Deposits, financial Institution, foreign capital. Cost Estimating, Cost Accounting, Fixed costs, variable costs selling price. (No Numericals)

(10 Hrs, 20 Marks)

Unit – IV
Manpower planning, factors affecting manpower planning sources of Recruitment, Need, objectives & benefits of Training, Method of Training workers, supervisors and Executives. Job Evaluation & Merit rating (Concept Only) Selling & Marketing Concept, Sales promotion, Advertising.

(10 Hrs, 20 Marks)

Unit – V
Quality (International Standard Organization of standards) ISO certificate Intellectual property rights (IPR), patents, Trademarks, copyrights, Management information system (MIS), Definition, Need & objectives of MIS, MIS & Computer, Designing of MIS, Application of MIS.

(10 Hrs, 20 Marks)

Reference Books –

1. Industrial Engineering & Production Management by M. Mahajan.
2. Engineering Management by Mazda, Pearson
3. Industrial Organization and Management by O.P. Khanna, Dhanpat Rai Publication
4. Management Information system by Jawdekar, THM
5. Information systems: Foundation of eBusiness by Alter, Pearson

6. Management by Stoner, Pearson

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TERM – I

ENGINEERING MATHEMATICS - III

Teaching Scheme:
Lectures: 4 Hrs / Week
Tutorial: 1 Hr / Week

Examination Scheme:
Theory Paper: 100 Marks (3 Hrs)
Term work: 25 Marks

Unit – I
Linear Differential Equation – Linear differential equation of order n, solution of LDE with constant coefficient, method of variation of parameters, equation reducible to linear form with constant coefficients, Cauchy's linear equation, Legendre's linear equation, Solution of simultaneous and symmetric simultaneous differential equation, applications to electric circuits.

(10 Hrs, 20 Marks)

Unit – II
Fourier and Z-transforms –
Fourier Transform (FT) – Fourier integral theorem, sine and cosine integrals, Fourier transform, Fourier cosine transform, Fourier sine transform and their inverses, Problems on wave equation.
Z-Transform – definitions, standard properties (without proofs), ZT of standard sequences and inverse, Solution of simple differential equations, Applications of Z-transform to discrete system analysis.

(10 Hrs, 20 Marks)

Unit – III
Laplace Transform (LT) – definition of LT, inverse LT, properties and theorems, LT of standard functions, LT of some special functions, (1^{st} order Bessel's periodic, unit step, unit impulses and ramp), Problems on finding LT and inverse LT, initial and final value theorems, applications of LT for network analysis.

(10 Hrs, 20 Marks)

Unit – IV
Statistics – mean, mode, median, standard deviation, variance, co-efficient of variation, Moments, skewness and kurtosis, Bivariate distribution, correlation and regression, reliability of regression estimates
Probability – Theorems on probability, Binomial distribution, Poisson distribution, Normal distribution

(10 Hrs, 20 Marks)

Unit – V
Probability – Beta distribution, Gamma distribution, Chi-square distribution
Theory of sampling – Sampling, types of sampling, sampling distribution, testing Hypothesis, Null hypothesis, level of significance, Test of significance, test of significance of large sample, decision quality control.

(10 Hrs, 20 Marks)

Text Books –

1. Advanced Engineering Mathematics – Erwin Kreyszig (Wiley Eastern Ltd)
2. Advanced Engineering Mathematics – H K Dass (S Chand)
3.

Reference Books –

1. Advanced Engineering Mathematics – Wylie C R and Barrett, McGraw Hill
2. Higher Engineering Mathematics – B S Grewal, Khanna Publication
3. Engineering Mathematics – B V Raman, Tata McGraw Hill
4. Applied Mathematics Vol 1 and 2 – P N Wartikar and J N Wartikar (Pune Vidharthi Griha Prakashan Pune)
5. Advanced Engineering Mathematics with MatLab, 2nd Edition – Thomas L Harman, James Dabney and Norman Richard, Thomson Learning
6. Engineering Mathematics – III – Dr. Gokhale, Dr. Chaudhary and Dr. Singh

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TERM – I

PROGRAMMING LABORATORY - I

Teaching Scheme:
Lectures: 3 Hrs / Week
Practical: 4 Hrs / Week

Examination Scheme:
Term work: 50 Marks
Practical: 50 Marks

Unit –I

Introduction to C - C Fundamentals, data types, constants, variables, Statements, operators, expressional, control statements.
Arrays - Representation and declaration of array one-dimensional array, two dimensional array, multidimensional array.
Strings - Representation, array of string, operation on sitting.
Pointers - Fundaments, declaration, advantage, pointers to different data types, array and pointers, array to pointers, operations on pointers
Functions - Need function definition, prototype, function, parameter, recursion, scope of Variables in the function, library functions, passing array to function, pointer to function

Unit – II

Structure - Definition, declaration, array to structures, structures within structures, structures, and function, structures and pointers, self-referential structures user defined data types – typedef.
Union - Need definition, operation, bit fields, difference between structure and union.
File Handling - Structure of file, file types, file operations
Macros - Substitution, File inclusion, complier, controlled directives.

Unit – III

Inter-conversion – Inter-conversion of Number system: decimal, binary, octal, hexadecimal.
System of liner equation - Gauss Elimination, Gauss Jordan, Jacobi or Gauss Siedel.
System of differential Equation - Taylor, Heun's method, Euler's modified method.

(10 Hrs, 20 Marks)

Unit – IV

Root of equations, Methods - Newton-Raphson, Raquel, faisi, Bolzano.
Interpolation - Newton backward, forward difference, table, divided difference.
Integration - Trapezoidal, Simpson's 1/3, 3/8 rules.

Unit – V

Permutation, Combination, powerset, Sorting - Insertion, Quick, Merge, Bubble, study of algorithms and implementation, analysis of sorting methods.
Searching - Linear search, binary search.

List of Laboratory Assignments -

1. Matrix Operation (Addition, Multiplication, Inverse)
2. Swapping of numbers using single pointer.
3. Processing student records using structure.
4. File manipulation opening closing, input and output operation files.
5. Program for macros.
6. Nesting of macro.
7. Macro with arguments
8. Inter conversion of number system.
9. To find value of unknown using Guass Elimination.
10. To find value of unknown using Guass Siedal.
11. To find root of equation using Newton Raphson.
12. To find root of equation using Regula-Falsi.
13. Find interpolating values using interpolation methods.
14. Find integral values using Simpson's 1/3, 3/8 rules.
15. Generation of Permutation for given list.
16. Generation of Combination for given list.
17. Generation of Power set.
18. String Operations.
19. Sorting using Bubble Sort.
20. Sorting using Quick Sort
21. Searching of given element using Linear search.
22. Searching of given element using Binary search.

The term work should include minimum 15 experiments from the above list.
The programs should be developed with integrated development environment (IDE) like Turbo C with emphasis on step-by-step development and debugging.

Reference Books -

1. M.K.Jain Iyanger "Numerical Method of Scientific and Engineering Computer" 3rd edition, New age publications.
2. E. Balaguruswami " programming in ANSI C" Tata McGraw Hill.
3. H. Schildt, " C The complete Reference" Tata McGraw Hill
4. Venugopal, K.R. and Prasad Sudeep R, "Programming With C" Tata McGraw Hill.
5. V. Rajaraman " Computer Oriented Numerical Methods" 3rd Edition Prentice Hall of India, Eastern Economy Edition.
6. Steven Chapra "Numerical Methods for Engineers" Tata McGraw Hill.
7. Ellis Horowitz and Sahani " Fundamentals of Data Structure" Tata McGraw Hill.
8. Kanetkar Y P, "Let us C" BPB Publications.

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TERM – II

MICROPROCESSOR - I

Teaching Scheme:
Lectures: 4 Hrs / Week
Practical: 2 Hrs / Week

Examination Scheme:
Theory Paper: 100 Marks (3 Hrs)
Term work: 25 Marks
Practical: 25 Marks

Unit – I

8086/ 8088 CPU architecture programming model Segmentation, Addressing modes, Instruction sets, Assembly language programming BIOS and DOS interrupts.

(10 Hrs, 20 Marks)

Unit - II

BIOS AND DOS Interrupts:, Introduction to DOS, Assembly language Programming in MSDOS using BIOS and DOS Interrupts, programming Technique, Time delay loop, produce and macros.

(10 Hrs, 20 Marks)

Unit – III

8086 Configuration:, Basic 8086 configuration, maximum and minimum modes, System bus timing, Interrupt priority management, programmable interrupt controller (PIC) 8259A 8089 (IOP)

(10 Hrs, 20 Marks)

Unit – IV

Main memory design: 8086 CPU Read/ Write timing SRAM and ROM interfacing requirement, address decoding technique full partial block PROM, Troubleshooting the memory module. DMA: Basic DMA operation, 8237 DMA Controller

(10 Hrs, 20 Marks)

Unit – V

Multiprocessor Configuration: Queue status and block facility 8086 based multiprocessor system, co-processor configuration, closely coupled configuration Overview of loosely coupled configuration, 8087 NDP, 8087 Data types and processor architecture, 8087 programming.

(10 Hrs, 20 Marks)

List of Experiments

Assembly language programming of 8086:

1. Study of BIOS and DOS interrupts
2. Study of MASM directives
3. Program for string manipulation
4. Program for password
5. HEX- BCD conversion
6. BCD- HEX conversion
7. BCD Addition
8. Program using MACRO
9. Program using NEAR procedure
10. Program using FAR procedure
11. Program to display Date and Time
12. Program using structures
13. Program using 8087 instruction set
14. Program using 8087 instruction set

The term work should include minimum 12 experiments. Program based on 8087 are compulsory.

Reference Book:

1. John E. Uffenbeck, “The 8086/ 8088 Family: Design, Programming and Interfacing, “ Pearson.
2. Douglas V. Hall “Microprocessor and Interfacing” Programming and Hardware” Pearson.
3. S.P. Dandomudi,“ Introduction to Assembly Language Programming – From 8086 to Pentium Processor” Springer.
4. Yu – Cheng Liu and Gleen A Gibson, “Microcomputer systems; The 8086 / 8088 Family Architecture, Programming and Design” 2nd Edition, Pearson.
5. Allen Wyatt, “Assembly Language Programming” QUE.
6. Peter Abel, “IBM PC Assembly Language and Programming” Pearson.
7. Barre B Brey “The Intel Microprocessor: 8085/ 8088, 80186/ 80286, 80386, 80186, Pentium, and Pentium Pro Processor- Architecture Programming and Interfacing” 4th Edition, Pearson.
8. A.K.Rai and K.M.Bhurchandi, “Advance Microprocessors and Principles- Architecture

Programming and Interfacing" Tata McGraw Hill.
9. B.Ram "Advanced Microprocessors and Interfacing", Tata McGraw Hill.

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TERM – II

DATA STRUCTURES AND FILES

Teaching Scheme:
Lectures: 4 Hrs / Week
Practical: 4 Hrs / Week

Examination Scheme:
Theory Paper: 100 Marks (3 Hrs)
Term work: 50 Marks
Practical: 50 Marks

Unit – I

Introduction: Concept of data, data types, data objects, structure, abstract data type, (ADT) and study. Implementation of data structure.

Stack and Queues: - Fundamental of stacks and queues, Data Structure of stack and queues, Basic operations on stacks and queues, Disadvantages and applications of stacks and queues, Concept of circular queues, basic operation on stacks and queues, Multi-stack and queues, priority queues.

Applications of Stacks:- Polish notation (infix, postfix, prefix) Evaluation of prefix and postfix expression , inter conversion of infix, prefix and postfix expression. Use of stack by function call and recursive function call, Multi-stack machines, Parenthesis matching, Towers of Hanoi, Queue application.

(10 Hrs, 20 Marks)

Unit – II

Linked list: Concept of Linked list, Basic Operations on a single linked list (Creation, insertion, deletion, traversing, concatenating, inverting and length finding) Linked stack and Queues, circular linked list, advantages of circular linked list, erasing circular linked list, Double linked list with basic operations like copy, storing polynomial using linked list, polynomial addition, and Generalized list, operations like copy, and equal depth on generalized list, Data representation for strings, pattern matching in string.

Storage Pool: - Initializing Storage Pool, allocating and (GETNODE) and deal locating (RET) a node Dynamic storage Management Procedure for allocation and freeing of blocks, First Fit, Best fit and Worst fit memory allocation Strategies.

(10 Hrs, 20 Marks)

Unit – III

Binary Tree: Basic terminology, Data structure and representation of binary tree, Binary tree traversal, and recursive and non recursive procedure for tree traversal, basic operations on binary tree, (Creation, insertion, deletion, printing, copy, equal and depth finding) Threaded binary tree, insertion in order threaded binary tree, In order traversal of in order threaded binary tree, Concept of binary search tree, Static tree labels, Huffman, Algorithms, Constructions, of optimal binary search tree, Dynamic tree tables, Basic Operation on it-insertion, deletion, height balanced binary tree, LL, LR, RL, RR Rotations

(10 Hrs, 20 Marks)

Unit – IV

Sorting - Algorithm for bubble sort, Insertion sort, Quick sort, selection sort, shell sort, merge sort, Heap sort, Radix sort, Radix exchange sort, Best average and worst case time complexity of each of the sorting and searching Algorithm

Hashing: Hashing function, overflow handling, collision, linear probing deletion, clustering re-

hashing bucket and chaining selection of good hash function

(10 Hrs, 20 Marks)

Unit – V

File Handing - Sequential and Relative Files: Description and organization, primitive operations on sequential and relative file.

Direct access file - Description and organization, primitive operations on direct access files

Indexed Sequential files and Indexes:-Description and organization, primitive operations on indexed sequential files, Indexed concept, linear indexes, tree indexes, algorithm for B-tree.

Multi Indexed files:- Description and organization of Inverted files, Multi list files, and algorithms for addition and deletion of records from the files.

(10 Hrs, 20 Marks)

List of Experiments

List of programming assignments to be developed in C/C++ with emphasis on developing debugging abilities

1. Implementation of stack using array or linked list
2. Implementation of Queue using array or linked list
3. Implementation of circular Queue using array or linked list
4. Conversion of Infix expression to postfix expression
5. Conversion of postfix expression to infix expression
6. Addition of two single variable polynomial using linked list
7. Implementation of double linked list and perform insertion, deletion and searching
8. Creation of binary tree and perform all non-recursive traversals.
9. Creation of binary search tree and perform insertion, deletion printing and in a tree shape.
10. Implementation of pattern matching in starting using linked listed.
11. Create a hash table and handle the collisions using liner probing with or without replacement.
12. Implementation of simple index file.
13. Insertion and deletion of a record from a direct access file using changing with and without replacement.
14. Insertion and deletion of a record from a sequential file.
15. Insertion and deletion of a record from a relative file
16. Insertion and deletion of a record from a multi list file

Term work should be minimum 12 experiments from the above list.

The programs should be developed with integrated development environment (IDE) like Turbo C with emphasis on step-by-step development and debugging.

Reference Books -

1. Ellis Horowitz and Sahani, “Fundamentals of data Structure” Galgotia.
2. Thomas R. Harborn, “ File system and Algorithms”, Prentice- Hall International
3. Trembaly and Sorenson “An Introduction to Data structures with Applications” Tata McGraw Hill.
4. Tannenbaum, “Data Structure C and C++, Pearson.
5. Sahani, “Data Structures, Algorithms and Applications in C++ McGraw Hill.
6. Seymour Lipschutz, “Data Structures”, Schaum’s Outline.
7. Weiss, “Data structure and Algorithm analysis in C”, Pearson

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TERM – II

COMPUTER ORGANIZATION

Teaching Scheme: Examination Scheme
Lectures: 4 Hrs / Week Theory Paper: 100 Marks (3 Hrs)

Unit – I

Introduction to system concepts: Functional Units, Basic operational concepts, instruction formats for machines, fixed and expanding opcodes, zero, two and three address schemes, concept of stack processor. General Addressing Modes.
Processor Organization: Instruction set design. 68000 architecture – Register structure and addressing modes, normal and exceptional processing. Bus structures.

(10 Hrs, 20 Marks)

Unit – II
Information representation, Big-endian and little-endian, data types, fixed and floating point representation, IEEE format for floating point and decimal algorithm, Booths algorithm, bit pairing methods, Restoring and non-restoring division algorithm. Floating point operations, guard bits and rounding

(10 Hrs, 20 Marks)

Unit – III
Control unit design, design levels, one / two / three bus CPU, hardwired control design methods and implementations, Microprogrammed control unit concepts and control unit design considerations, Wilkes design, Nano programmed computers, bit-slice architecture, 2900 family CPU designs, emulation.

(10 Hrs, 20 Marks)

Unit – IV
Memory Organization: Memory hierarchies, memory interleaving, cache memories organization, virtual memory and organization, performance considerations, content addressable memories, memory management in 68000 family and cache designs, Introduction to SRAM, DRAM, RDRAM, Flash memory.

(10 Hrs, 20 Marks)

Unit – V
System Organization: Buses, interconnection system bus, CPU and IO bus-bus operation, UNIBUS, multibus and IEEE 488 I/O addressing, data transfer, synchronization, serial and parallel ports, I/O interfaces, I/O channel, PCI bus, SCSI bus, Universal Serial Bus. RISC architecture, concepts, CISC versus RISC, advantages of RISC

(10 Hrs, 20 Marks)

Reference Books –

1. Hamacher, Vransic, Zaky, “Computer Organization”, 5th Ed., McGraw Hill international.
2. J. P. Hayes, “Computer Architecture and Organization”, 3rd Ed. McGraw Hill international.
3. Tanenbaum, “Structured Computer Organization”, Pearson.
4. William Stallings, “Computer Organization And Architecture”, 6th ed., Pearson.
5. Nicholas Carter, “Computer Architecture”, Schaum’s Outline.

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TERM – II

DIGITAL SYSTSEM DESIGN

Teaching Scheme: Examination Scheme
Lectures: 4 Hrs / Week Theory Paper: 100 Marks (3 Hrs)

Unit – I

Combinational Logic Design: Using MSI circuits, BCD Adder, BCD subtractor, BCD to 7-segment decoder, Adder / Subtractor using IC 7483.
Design of code Converter circuits: BCD to Binary, Binary to BCD, BCD to Gray, Gray to BCD, BCD to Ex-3, Etc.
Design of counter and shift register using IC 7493 & IC 7495.

(10 Hrs, 20 Marks)

Unit – II
Design of ROM, PLA, PAL: Basic structure of ROM, size of Rom, Design of ROM, Structure of PLA, PAL, and their designs. Introductions to complex programmable Logic devices (CPLDs) & Field – Programmable Gate Array, (FPGA)

(10 Hrs, 20 Marks)

Unit – III
Sequential Logic Design:- Review of excitation table of S-R, J-K, D & T flip-flops. Analysis of clocked sequential circuit state table, state diagram, next stat equations, state reduction, state assignment. Design of register, shift resistor ripple counter, synchronous counters, sequence generator & detector.

(10 Hrs, 20 Marks)

Unit – IV
Asynchronous sequential circuit: Asynchronous verses Synchronous sequential circuit, Application of Asynchronous sequential circuit.
Asynchronous sequential Machine modes, Analysis of Asynchronous sequential Machine, Design of Asynchronous Sequential circuit

(10 Hrs, 20 Marks)

Unit – V
Algorithmic state Machines.
ASM chart, definition, standard symbols for ASM chart Method of implementation ASM chart by 'D' Flip Flop, Mux – Controller, Rom Controller, One hot controller.
Generation of ASM chart for different waveforms, Miscellaneous problem of ASM chart, e.g. Traffic light, Washing machine, Wending machine etc.
Introduction to VHDL: Entity, Architecture, configuration Declaration Generic, Data objects example of VHDL codes.

(10 Hrs, 20 Marks)

Reference Books –

1. "Modern Digital Electronics" by R.P. Jain, 3rd Edition, TMH.
2. "Digital Logic and Microprocessor" by F.J. Hill, John Willy & sons.
3. "Digital Electronic circuit and system" by V.K.Puri, TMH.
4. "Digital Design" by M. Morris Mano, Pearson.

TERM – II

DATA COMMUNICATION

Teaching Scheme: Examination Scheme
Lectures: 4 Hrs / Week Theory Paper: 100 Marks (3 Hrs)

Unit – I
Introduction to data communication and networks –
Data communication – Components, data representation, direction of flow
Networks – network criteria, network hardware, network software, protocol hierarchy, design issues for the layer, ISO OSI reference model
Signals – Analog signals, digital signal, analog verses digital signal, data rate limits, transmission impairment, throughput, propagation speed, propagation time, wavelength etc.

(10 Hrs, 20 Marks)

Unit – II
Digital transmission and analog transmission –
Digital transmission – line coding, characteristics, schemes. Block coding, transformation and common block codes. Sampling – PAM, PCM, Nyquist's theorem, bit rate, transmission modes.
Analog transmission – Analog modulation, AM, FM, PM. Digital modulation, ASK, FSK, PSK, QAM. Bit/baud comparison.
Telephone modems – Modem standards, traditional modems, 56K modems etc.

(10 Hrs, 20 Marks)

Unit – III
Multiplexing – FDM – Multiplexing process, de-multiplexing process, applications of FDM, WDM, TDM – Time slots, frames, interleaving, synchronization, bit padding, DSS, T-Lines, inverse TDM, Applications of TDM.
Transmission media – Guided media, twisted pair, coaxial cable, fiber optics, unguided media, radio waves, microwaves and infrared.
Switching – Circuit switching, packet switching and message switching. Telephone networks – components, LATAs, making conections, analog services and digital services.

(10 Hrs, 20 Marks)

Unit – IV
Error detection and correction –
Types of errors, single bit burst errors. Detections – redundancy, parity, CRC, checksum. Error correction – Correction by retransmission, FEC, Burst error correction.
Flow control and error control – stop and wait ARQ, Go-back-N ARQ, selective repeat ARQ.

(10 Hrs, 20 Marks)

Unit – V
Ethernet – Traditional Ethernet, fast Ethernet, gigabit Ethernet.
Multiple access – random access, MA, CSMA, CSMA/CD, CSMA/CA, control access, FDMA, TDMA, and CDMA.
IEEE 802.3, 802.4, 802.5, X.21, X.25, SDLC/HDLC protocol standards.
Introduction to network connecting devices – repeater, bridge, router, gateway, hub etc.

(10 Hrs, 20 Marks)

Reference Books –

1. "Computer Networks" A S Tanenbaum 4th edition, Pearson
2. "Data Communication and Networking" B Forouzan, 3nd edition, TMH
3. "Data Communication and Networking" Achyut Godbole, TMH

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TERM – II

PROGRAMMING LABORATORY - II

Teaching Scheme:
Lectures: 2 Hrs / Week
Practical: 4 Hrs / Week

Examination Scheme:
Term work: 50 Marks
Practical: 50 Marks

Unit – I

Introduction to Object Oriented Programming - Need of Object Oriented Programming:
A look at Procedure Oriented Programming, Object Oriented Programming Paradigm
Basic Concept of OOP - Objects, classes, Data Abstraction, Encapsulation, Inheritance, Polymorphism, Data hiding ,Message Passing. Benefits of OOP, Application of OOP

Beginning with C++ : What is C++, Structure of C++ Program, A simple C++ program, comments, output using Count, input using Cin, declaration of variables, Reference variables, Token, Keywords, Identifier, Constant, Basic data types, Derived data types.

Unit – II

Control structures , Classes and Objects - Control Structures: If statement, switch statement, Do while statement, while statement and For statement.
Classes and objects: Specifying a Class, Defining Member function, A C++ program with class, Nesting of member function, Private member function, Array within a class, memory allocation for objects, Static Data member, Static member function, Array of Objects, Objects as function argument, Friendly function, Returning objects.
Constructor and destructor - Constructor Parameterized Constructor, Multiple Constructor in a class, Constructor with default argument, Dynamic Initialization of Objects,
Copy Constructor, Destructor

Unit – III

Functions and Operator overloading - Function in C++: The main function, Function prototype, Call by value, Call by reference, Return by reference, Inline Function, Default Argument, Function Overloading,
Operator - Operator in C++, Scope Resolution Operator, Operator Precedence
Operator Overloading - Defining Operator overloading, Overloading Unary Operator, Overloading Binary operator, Overloading binary operator using friend, Rules for operator overloading
Type conversion

Unit – IV

Inheritance and Pointer, Virtual function and Polymorphism, Inheritance: Introduction, Defining Derived classes, Single inheritance, Making a Private member inheritable, Multilevel Inheritance, Multiple Inheritance, Hierarchical Inheritance, Hybrid inheritance, Virtual base classes, Abstract classes, Constructor in derived class.
Pointer, Virtual Function and Polymorphism: Introduction, Pointer to Object, this pointer, Pointer to Derived classes, Virtual function.

Unit – V

Managing Console I/O operation and File Operation - Managing Console I/O operation: C++ Stream, C++ Stream Classes, Unformatted I/O Operation, Formatted Console I/O operation, Managing Output with manipulators
Working with files: Classes for File Stream Operations, Opening and Closing a File, Detecting End Of File, More about Open (): File Modes, File Pointer and their manipulator, Sequential Input

and Output Operations, Updating a File: Random Access. Error handling during file operation, Template: Function template, Class Template

Laboratory Assignment: -

1. One Simple C++ Program
2. C++ Simple Program using Control Structure.
3. Program to create array of Object.
4. Program that illustrate use of various types of constructor
5. Program for String Manipulation
6. Program for Unary Operator Overloading.
7. Program for Binary Operator Overloading
8. Program for Function Overloading
9. Program for Multilevel inheritance
10. Program for Run time polymorphism using Virtual Function
11. Program to format output using manipulator
12. Program for File Handling
13. Program using Template
14. Mini project in C++ (e.g. Banking system, Railway reservation system etc.)
15. Program for stack operations using class
16. Program for Queue operations using class

Term work should include minimum 12 experiments from the above list.
The programs should be developed with integrated development environment (IDE) like Borland C++ with emphasis on step-by-step development and debugging.

Reference Books –

1. E. Balgurusamy," Object Oriented Programming with C++ ", III Edition TATA McGraw –Hill Publication
2. Kanetkar Y. , " Let Us C++" , BPB Publication
3. Schildt, " C++ The Complete Reference ", Tata McGraw Hill Publication.